CLAIMS

1. A microcomputer having a real-time trace function, said microcomputer comprising:

a central processing unit for executing an instruction;

instruction address setting means for setting an instruction address for detecting an execution of a plurality of instructions to be executed by said central processing unit; and

detection signal output means for outputting a detection signal through a single detection signal output terminal, when the execution of said plurality of instructions has been detected.

2. The microcomputer as defined in claim 1, wherein:

said plurality of instructions comprises a first instruction and a second instruction, and

said detection signal output means omits outputting a detection signal when said first instruction is successively executed after said first instruction is executed and a detection signal is output, and outputs a detection signal only when said second instruction is executed.

3. The microcomputer as defined in claim 1, further comprising:

status information output means for outputting status information indicating an execution state of said central processing unit to a status information output terminals,

wherein one of said status information output terminals is also used as said detection signal output terminal.

4. The microcomputer as defined in claim 2, comprising:

status information output means for outputting status information indicating an execution state of said central processing unit to a status information output terminals,

wherein one of said status information output terminals is also used as said detection signal output terminal.

5. The microcomputer as defined in claim 3,

wherein said status information comprises information for identifying to which of the following states the execution state of said central processing unit belongs: ordinary instruction execution, relative branch instruction execution, absolute branch instruction execution, a match with said instruction address during ordinary instruction execution, a match with said instruction address during relative branch instruction execution, and a match with said instruction address during absolute branch instruction execution.

6. The microcomputer as defined in claim 1,

wherein an instruction address that is set by said instruction address setting means comprises an address for specifying at least one of start and end of a trace range.

7. The microcomputer as defined in claim 2,

wherein an instruction address that is set by said instruction address setting means comprises an address for specifying at least one of start and end of a trace range.

8. The microcomputer as defined in claim 5,

wherein an instruction address that is set by said instruction address setting means comprises an address for specifying at least one of start and end of a trace range.

9. The microcomputer as defined in claim 1,

wherein an instruction address that is set by said instruction address setting means comprises an address for specifying at least one of a start and end of a execution-time measurement range of a program.

10. The microcomputer as defined in claim 2,

wherein an instruction address that is set by said instruction address setting means comprises an address for specifying at least one of a start and end of a execution-time measurement range of a program.

11. The microcomputer as defined in claim 5,

wherein an instruction address that is set by said instruction address setting means comprises an address for specifying at least one of a start and end of a execution-time measurement range of a program.

12. The microcomputer as defined in claim 6,

wherein an instruction address that is set by said instruction address setting means comprises an address for specifying at least one of a start and end of a execution-time measurement range of a program.

13. The microcomputer as defined in claim 1, wherein:

said instruction address setting means comprises a plurality of registers for holding instruction address information for detecting the execution of a plurality of instructions, and

said detection signal output means comprises:

means for holding a comparison result between an instruction address that was read out previously for instruction execution by said central processing unit and an address that has been held in each of said registers, until the instruction at said previously read-out instruction address is executed, and outputting a detection signal based on said held comparison result when said instruction at said previously read-out instruction address has been executed; and

means for invalidating said comparison result with instructions that were read out before said branch instruction was executed when said executed instruction was a branch instruction.

14. The microcomputer as defined in claim 7, wherein:

said instruction address setting means comprises a plurality of registers for holding instruction address information for detecting the execution of a plurality of instructions, and

said detection signal output means comprises:

means for holding a comparison result between an instruction address that was read out previously for instruction execution

by said central processing unit and an address that has been held in each of said registers, until the instruction at said previously read-out instruction address is executed, and outputting a detection signal based on said held comparison result when said instruction at said previously read-out instruction address has been executed; and

means for invalidating said comparison result with instructions that were read out before said branch instruction was executed when said executed instruction was a branch instruction.

15. The microcomputer as defined in claim 10, wherein:

said instruction address setting means comprises a plurality of registers for holding instruction address information for detecting the execution of a plurality of instructions, and

said detection signal output means comprises:

means for holding a comparison result between an instruction address that was read out previously for instruction execution by said central processing unit and an address that has been held in each of said registers, until the instruction at said previously read-out instruction address is executed, and outputting a detection signal based on said held comparison result when said instruction at said previously read-out instruction address has been executed; and

means for invalidating said comparison result with instructions that were read out before said branch instruction was executed when said executed instruction was a branch

instruction.

16. The microcomputer as defined in claim 13, wherein:

said registers comprise at least two registers for holding a start address and an end address for defining a given range of a program, and

said detection signal output means comprises:

first comparison means and second comparison means for comparing an instruction address, that was read out previously for instruction execution by said central processing unit, with said start address and said end address;

a comparison result holding section that is capable of holding a plurality of comparison results from said first comparison means and said second comparison means;

means for reading said comparison results held in said comparison result holding section, at a timing that said previously-read instruction has been executed;

means for resetting any said comparison results held in said comparison result holding section when an executed instruction was a branch instruction; and

a logic circuit for outputting a detection signal based on said comparison results that have been read from said comparison result holding section, when addresses that are held in said first register and said second register have been executed in a predetermined sequence.

17. The microcomputer as defined in claim 14, wherein:

said registers comprise at least two registers for holding

a start address and an end address for defining a given range of a program, and

said detection signal output means comprises:

first comparison means and second comparison means for comparing an instruction address, that was read out previously for instruction execution by said central processing unit, with said start address and said end address;

a comparison result holding section that is capable of holding a plurality of comparison results from said first comparison means and said second comparison means;

means for reading said comparison results held in said comparison result holding section, at a timing that said previously-read instruction has been executed;

means for resetting any said comparison results held in said comparison result holding section when an executed instruction was a branch instruction; and

a logic circuit for outputting a detection signal based on said comparison results that have been read from said comparison result holding section, when addresses that are held in said first register and said second register have been executed in a predetermined sequence.

18. The microcomputer as defined in claim 15, wherein:

said registers comprise at least two registers for holding a start address and an end address for defining a given range of a program, and

said detection signal output means comprises:

first comparison means and second comparison means for

comparing an instruction address, that was read out previously for instruction execution by said central processing unit, with said start address and said end address;

a comparison result holding section that is capable of holding a plurality of comparison results from said first comparison means and said second comparison means;

means for reading said comparison results held in said comparison result holding section, at a timing that said previously-read instruction has been executed;

means for resetting any said comparison results held in said comparison result holding section when an executed instruction was a branch instruction; and

a logic circuit for outputting a detection signal based on said comparison results that have been read from said comparison result holding section, when addresses that are held in said first register and said second register have been executed in a predetermined sequence.

19. Electronic equipment comprising:

the microcomputer as defined in claim 1;

an input source of data that is to be processed by said microcomputer; and

an output device for outputting data that has been processed by said microcomputer.

20. Electronic equipment comprising:

the microcomputer as defined in claim 7;

an input source of data that is to be processed by said

microcomputer; and

an output device for outputting data that has been processed by said microcomputer.

21. Electronic equipment comprising:

the microcomputer as defined in claim 10;

an input source of data that is to be processed by said microcomputer; and

an output device for outputting data that has been processed by said microcomputer.

22. A debugging system for a target system that comprises a microcomputer, wherein:

said microcomputer comprises:

a central processing unit for executing an instruction;

instruction address setting means for setting an instruction address for detecting an execution of a plurality of instructions to be executed by said central processing unit; and

detection signal output means for outputting a detection signal through a single detection signal output terminal, when the execution of said plurality of instructions has been detected, and

said debugging system further comprises:

trace information acquisition means for receiving said detection signal from said microcomputer, and acquiring trace information by controlling a start and end of the acquisition of trace information, based on said detection signal.

23. A debugging system for a target system that comprises a microcomputer, wherein:

said microcomputer comprises:

a central processing unit for executing an instruction;

instruction address setting means for setting an instruction address for detecting an execution of a plurality of instructions to be executed by said central processing unit; and

detection signal output means for outputting a detection signal through a single detection signal output terminal, when the execution of said plurality of instructions has been detected, and

said debugging system further comprises:

execution-time measurement means for receiving said detection signal from said microcomputer, and measuring execution time by controlling a start and end of measurement of program execution time, based on said detection signal.

24. The debugging system as defined in claim 22, wherein:

said plurality of instructions comprises a first instruction and a second instruction, and

said detection signal output means omits outputting a detection signal when said first instruction is successively executed after said first instruction is executed and a detection signal is output, and outputs a detection signal only when said second instruction is executed.

25. The debugging system as defined in claim 23, wherein:

said plurality of instructions comprises a first

instruction and a second instruction, and

said detection signal output means omits outputting a detection signal when said first instruction is successively executed after said first instruction is executed and a detection signal is output, and outputs a detection signal only when said second instruction is executed.